REMARKS

This Response seeks to place this application in condition for allowance. All of the Examiner's rejections have been addressed below. Claims 1-24 and 26-37 are pending. Claim 25 was cancelled, without prejudice, in a previous amendment. Claims 1 and 23 have been amended. No new matter has been added.

Office Action

In the non-final Office Action dated July 18, 2002 (hereinafter, "OFFICE ACTION"), the Examiner rejected claims 1-11, under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,329,694 to Lee et al. (hereinafter, "Lee"). Furthermore, claims 12-22, 28, and 31-37 were rejected under 35 U.S.C. §103(a) as being "unpatentable" over Lee. Finally, claims 23, 24, 26, 27 and 30 were rejected under 35 U.S.C. §103(a) as being "unpatentable" over Lee in view of a Japanese patent to Sakai et al. (hereinafter, "Sakai").

Applicants submit that independent claims 1, 12, and 23 are neither anticipated nor rendered obvious by Lee. It should be noted that, although not separately addressed herein, dependent claims 2-11, 13-22, 24, and 26-37 incorporate limitations that present patentable subject matter in their own right. However, in an attempt to present a more concise response to the OFFICE ACTION, only certain limitations or elements of independent claims 1, 12 and 23 are discussed below. No inference or conclusion of any kind should be drawn from the absence of comments pertaining to other limitations or elements, whether those limitations or elements are contained in independent or dependent claims.

Claim 1 is not Anticipated by Lee

In the OFFICE ACTION, claim 1 was rejected as being anticipated by Lee. Applicants respectfully submit that independent claim 1 (in its amended or pre-amended form) is not anticipated by Lee. Claim is directed toward an integrated circuit device and (as amended) recites, in part:

> **a bond pad structure including:**
>
> a conductive pad;
>
> a first doped region of a first conductivity type disposed in a semiconductor substrate of a second conductivity type, wherein the first doped region is underlying and surrounding the conductive pad;
>
> a conductive region of the first conductivity type disposed in the first doped region;
>
> a first tap region spaced apart from and surrounding a substantial portion of the first doped region, wherein the first tap region is electrically coupled to a first supply voltage;

Regarding claim 1, the Examiner states that "Lee discloses, figure 14, an integrated circuit device comprising: a conductive pad (I/O pad)... a first doped region ... underlying and surrounding the conductive pad" (OFFICE ACTION, page 2, item 2). In the section titled "Response to Arguments" (page 7 of the OFFICE ACTION, item 6), the Examiner also states that (in Lee) "n-well 61 is underlying, and at least surrounding the lower portions of the "I/O pad" (the "n-well 61" being part of a transistor structure).

Applicants respectfully believe this is a mischaracterization of Lee and is counter to what is actually disclosed in Lee. In Lee, there is no disclosure or detail regarding any physical structure of the "I/O pad", much less any "lower portion" of the "I/O pad". Lee, in Fig. 14, at the very most only demonstrates, schematically, that the "I/O pad" is coupled to the transistor. Such

a schematic representation does not provide any information about the physical characteristics of the bond pad or its physical position with respect to a doped region as claimed.

In Lee, the I/O pad, is mentioned extensively throughout the patent as an "I/O pad", "data output pad", or "data input pad"[1], but is never described in any detail in terms of form, structure or placement relative to the substrate ("p-sub", Fig. 14). However, there is no indication that the I/O PAD is in any way different from a conventional bond pad structure, for example, such as the one described in the BACKGROUND OF THE INVENTION section of the instant application on page 4 line 8 to page 4 line 18, and Figure 2B, i.e.,

> [The conventional bond pad includes a] conductive bond pad layer 210, formed on a semiconductor substrate 230 ... disposed above the doped region 220 [which] typically includes an impurity region of opposite conductivity type than that of the substrate 230. This impurity region forms a PN junction with the substrate 230 to prevent or minimize the possibility of a short circuit between the bond pad layer 210 and the substrate 230.

The transistor structure, e.g., such as the one shown in Lee, includes a doped region (e.g., "n-well 61", Fig. 14) disposed in the substrate ("p-sub, Fig. 14) that would need to be apart and isolated from the doped region 220 of the conventional bond pad structure described above. That is, these structures require dedicated doped regions located physically apart from each other.

It should be noted that Applicants have amended claim 1 to more particularly claim the subject matter by adding "a bond pad structure". As mentioned above, Lee neither discloses or suggests a bond pad structure having the elements recited in claim 1. Thus, for at least these reasons, Applicants submit that claim 1 is not anticipated by Lee.

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[1] Unless specified otherwise, "I/O pad", "data input pad", and "data output pad", as they are referred to in Lee, shall be collectively referred to hereinafter as "the I/O PAD".

Claim 12 is not Obviated by Lee

In the OFFICE ACTION, claim 12 was rejected as being obvious in view of Lee. Claim 12 is directed to a bond pad for an integrated circuit device and recites in part:

> the bond pad comprising:
>
> a conductive bonding layer;
>
> a doped region of a first conductivity type formed in a semiconductor substrate of a second conductivity type, wherein the doped region is underlying and surrounding the conductive bonding layer;
>
> a conductive region of the first conductivity type disposed in the doped region, wherein the conductive region is underlying the conductive bonding layer and wherein the conductive region includes a surface area at least substantially equal to a surface area of the conductive bonding layer; and
>
> a conductive tap region spaced apart from and surrounding at least a portion of the doped region, wherein a portion of the conductive tap region is electrically coupled to a supply voltage.

Applicants respectfully submit that claim 12 is not rendered obvious by Lee. In the OFFICE ACTION, the Examiner stated, "Lee discloses the bond pad comprising bonding layers 63-65... a conductive region 65 of the first conductivity type disposed in the first doped region..." Applicants respectfully submit that this statement is a mischaracterization in that Lee, in Fig. 14, simply illustrates sectional views of common transistor structures which do not form any part of a bond pad. For example, the "bonding layers 63-65" mentioned above cannot be a "conductive bonding layer" of a bond pad as prescribed in claim 12. Rather, the "bonding layers 63-65" are in fact a source region (63, Fig. 14), a drain region (64, Fig. 14), and a p+ pickup region (65) of the conventional transistor structure.

Lee, in Fig. 14 as explained above with respect to claim 1, simply illustrates sectional views of common transistor structures schematically coupled to an I/O PAD, and do not convey

any placement of the I/O PAD relative to the transistor structure. There is no indication that the I/O PAD of Lee is in any way different from a conventional bond pad structure. Such a conventional bond pad structure would be located apart from the transistor formed in n-well 61 (and not reside above the doped region 61).

In the OFFICE ACTION, the Examiner has stated:

> Lee does not disclose the surface region substantially equal to the surface area of the conductive bonding layer. It would have been within the level of ordinary skill in the art to change the size of region 65.

Applicants respectfully submit that it would be counterintuitive to change the surface area of the "p+ pickup region 65" as stated in the OFFICE ACTION and arrive at the bond pad as claimed in claim 12. To change the surface area of the the "p+ pickup region 65" of Lee would only produce a transistor structure having a "p+ pickup region 65" of differing size. As is described above, the I/O PAD (again, although structurally not disclosed) would need to be a separate, isolated structure from the "p+ pickup region 65" of the transistor structure shown in Fig. 14.

Thus, for at least these reasons, Applicants submit that claim 12 is not anticipated or rendered obvious by Lee.

Claim 23 is not Obviated by Lee in view of Sakai

In the OFFICE ACTION, claim 12 was rejected as being obviated by Lee in view of Sakai. Claim 23 is directed to a transistor layout and, as amended, recites in part:

> a conductive tap region spaced proximal to and surrounding the drain region, wherein the conductive tap region is electrically coupled to a supply voltage and electrically and physically coupled to the source region, wherein a section of the

conductive tap region is structurally integrated with the source region.

Applicants respectfully submit that independent claim 23 is not rendered obvious by Lee either by itself or in view of Sakai. In the OFFICE ACTION, the Examiner stated "it would be obvious to one of ordinary skill in the art to make the source and the drain region of the opposite conductivity type since it was known in the art that both conductivity types could be present in source/drain region (see the Japanese patent figure 4c)".

Applicants respectfully submit that it would not be obvious to make the source (63, Fig. 14) of the transistor structure disclosed in Lee to include a second conductivity type and the drain region to include a first conductivity type in view of Sakai, because Sakai, does not disclose or suggest a transistor having a source (or drain) region with both first and second conductivity types. Sakai, to the extent understood, is directed to a Read-Only Memory ("ROM") whose memory cell transistors include "isolation regions" to isolate source and drain regions from gate regions. These "isolation regions" are disposed between the gate and the source/drain regions and are used to isolate the source and drain regions from the gate region to selectively program those memory cell transistors, for example: "memory information is written in by the selection of the kind of the conductivity type of impurity regions between the source and drain regions, 1, 2, 7, 8 and the gate regions", see the English document attached to Sakai as provided in the OFFICE ACTION, section titled "CONSTITUTION". See also, the section titled "ABSTRACT" of the English document, i.e, "To realize an ROM ... by isolating the source and drain regions of a MOS transistor from the gate region, and forming an impurity region in the isolation region".

It should be noted that Applicants have amended claim 23 to more particularly claim the subject matter by including that "a section of the conductive tap region is structurally integrated

with the source region". Applicants respectfully submit that Lee, by itself or in combination with Sakai, does not include, among other things, a transistor layout that includes a section of a conductive tap region which is structurally integrated with the source region.

No new matter has been added. This amendment to claim 23 is fully disclosed in the specification, for example, see page 20, lines11-20.

Conclusion

Applicants request reconsideration of the instant application in view of the foregoing remarks and amendments. Applicants submit that the pending claims present patentable subject matter. Accordingly, allowance of all of the claims is respectfully requested.

The Examiner is invited to contact the undersigned if a telephone call could help resolve any remaining issues

Respectfully submitted,

Date: Oct 18, 2002

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Exhibit A – Version With Markings to Show Changes Made to The Claims

1. **(Thrice Amended)** An integrated circuit device comprising:

a bond pad structure including:

a conductive pad [to receive an input signal from an external signal line];

a first doped region of a first conductivity type disposed in a semiconductor substrate of a second conductivity type, wherein the first doped region is underlying and surrounding the conductive pad;

a conductive region of the first conductivity type disposed in the first doped region;

a first tap region spaced apart from and surrounding a substantial portion of the first doped region, wherein the first tap region is electrically coupled to a first supply voltage;

an output driver transistor having a drain region and a source region, wherein the drain region is electrically coupled to the conductive pad; and

a second tap region surrounding the output driver transistor, wherein the second tap region is electrically and physically coupled to a second supply voltage and the source region.

23. **(Thrice Amended)** A transistor layout for an integrated circuit device having a bond pad, the transistor layout comprising:

a drain region having a first conductivity type doping, wherein the drain region is formed in a semiconductor substrate region having a second conductivity type doping, the drain region being electrically coupled to the bond pad;

a source region including a second conductivity type doping; and

a conductive tap region spaced proximal to and surrounding the drain region, wherein the conductive tap region is electrically coupled to a supply voltage and electrically and physically coupled to the source region, wherein a section of the conductive tap region is structurally integrated with the source region.